



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 10/025,437 Confirmation No.: 6542
First Named Inventor: Soltan Filing Date: 2001/12/18
Group Art Unit: Examiner:
Atty. Docket No.: M-12367 US
Title: INTERNAL IMPEDANCE MATCH IN INTEGRATED CIRCUITS
Assignee: Tavanza Inc.

Half Moon Bay, California
August 14, 2003

COMMISSIONER FOR PATENTS
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Submitted by first class mail and FAX 1 703 305 8568

REQUEST FOR CORRECTED PUBLICATION OF PATENT APPLICATION

Dear Sir:

Hereby requested is correction of the publication of the above-identified patent application.

This request is submitted for the following reason(s):

The published Abstract, Claims and specification appear to be those of an unrelated patent application.

For the office's convenience, a sample page of the correct claims is attached hereto.

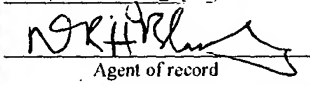
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Application No. 10/025,437

Because this was not an error on the part of Applicant(s), Applicant(s) believe no fee is required.

If there are any queries arising, please contact the undersigned at (650) 726 3841, Pacific Time.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA on

14 August 2003.

Agent of record
Date of Signature 14 August 2003

Respectfully submitted,



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- 1 1. An integrated circuit comprising:
 - 2 an amplifier formed on a semiconductor die, the amplifier having an
 - 3 output port with an output impedance; and
 - 4 a bondwire electrically connecting the output port to an external
 - 5 conductor;
 - 6 wherein the bondwire has a specified self-inductance and is operable to
 - 7 match the output impedance to a desired load impedance.
- 1 2. The integrated circuit of claim 1 wherein:
 - 2 the amplifier is a radio frequency power amplifier.
- 1 3. The integrated circuit of claim 1 wherein:
 - 2 the semiconductor die is a metal-oxide semiconductor die.
- 1 4. The integrated circuit of claim 1 wherein:
 - 2 the semiconductor die is a gallium arsenide semiconductor die.
- 1 5. The integrated circuit of claim 1 wherein:
 - 2 the semiconductor die is a bipolar semiconductor die.
- 1 6. A method for impedance matching comprising:
 - 2 forming an amplifier on a semiconductor die, the amplifier having an
 - 3 output port with an output impedance; and
 - 4 connecting an electrically conducting bondwire between the output port
 - 5 and an external conductor;